Amendments to the Claims:

Please amend claims 71-75 and 79-84 as shown in the following listing of claims. This listing of claims will replace all prior versions and listings of claims in the application:

1-70. (cancelled)

71. (currently amended) An integrated circuit communication device configured for operation over a multi-pair transmission channel, the communication device comprising:

a ~~decision feedback sequence estimation (DFSE) circuit~~ trellis decoder adapted to decode an input sample into a final decision corresponding to a codeword of a trellis code ~~having N states, the DFSE including a single state decision feedback equalizer~~;

an intersymbol interference (ISI) compensation circuit configured to compensate for an ISI component;

adaptive circuitry ~~adapted~~ operable to reduce power consumption of a filter~~, the filter having an initial set of active coefficients, an input and an output, the active coefficients being ordered, a lowest ordered active coefficient of the initial set being proximal to the input, each of the active coefficients having a stable value~~ having a plurality of taps, the adaptive circuitry operable to one of activate and deactivate selected taps of the filter based on an error metric and a power metric.

72. (currently amended) The integrated circuit communication device according to claim 71, wherein each tap of the filter has an associated coefficient, wherein the adaptive circuitry is operable to compare the coefficient associated with a given tap to a threshold value and wherein the adaptive circuitry is operable to one of activate and deactivate the given tap based on said comparison ~~further comprising:~~

~~a threshold module generating a threshold;~~

~~a comparing module coupled to the threshold module, the comparing module comparing an active coefficient with the threshold; and~~

~~a decision module coupled to the comparing module, the decision module deactivating the active coefficient according to a criterion~~.

73. (currently amended) The integrated circuit communication device according to claim 72, wherein the ~~decision module~~ adaptive circuitry is operable to deactivate~~s~~ the ~~active coefficient~~ given tap if the ~~active~~ coefficient has a value smaller than the threshold.

74. (currently amended) The integrated circuit communication device according to claim 73, further comprising:

~~a buffer providing a specified error;~~

an error computing module computing ~~an~~ the error metric; and

~~a second comparing module coupled to the buffer, the error computing module and the threshold module, the second comparing module comparing~~ wherein the adaptive circuitry is operable to compare the error metric with ~~the~~ a specified error ~~and producing a first control signal to the threshold module when the error metric is smaller than the specified error and a second control signal to the threshold module when the error metric is larger than the specified error~~.

75. (currently amended) The integrated circuit communication device according to claim 74, wherein the ~~threshold module~~ adaptive circuitry is operable to update~~s~~ the threshold ~~upon reception of the first or second control signal~~ based on the comparison of the error metric with the specified error.

76. (previously presented) The integrated circuit communication device according to claim 71, wherein the ISI compensation circuit comprises:

an inverse partial response filter having an impulse response substantially an inverse of an impulse response of a pulse shaping filter of a remote transmitter, so as to substantially compensate an input digital signal for an ISI component.

77. (original) The integrated circuit communication device according to claim 76, wherein the inverse partial response filter is implemented with a characteristic feedback gain factor K.

78. (original) The integrated circuit communication device according to claim 77, wherein the inverse partial response filter operates in accordance with a non-zero value of the characteristic feedback gain factor K during communication initialization and wherein the value of the feedback gain factor K is ramped down to zero after a pre-defined interval.

79. (currently amended) The integrated circuit communication device according to claim 71, wherein the ISI compensation circuit comprises:

~~a Viterbi decoder configured to decode a digital signal and generate tentative decisions; and~~

feedback equalizer circuitry coupled to the ~~Viterbi~~ trellis decoder, the feedback equalizer circuitry receiving ~~the~~ tentative decisions from the trellis decoder and combining the tentative decisions with a set of high-ordered coefficients to generate a first value.

80. (currently amended) The integrated circuit communication device according to claim 79, wherein the intersymbol interference (ISI) compensation circuit further comprises:

summing circuitry combining the first value with a digital signal, the summing circuitry outputting an intermediate signal; and

a multiple decision feedback equalizer receiving the intermediate signal and combining the intermediate signal with a set of pre-computed values generated by combining values of a set of low-ordered coefficients with a set of values representing levels of a multi-level symbolic alphabet to produce a set of potential digital signals, one of the potential digital signals being substantially ISI compensated, the multiple decision feedback equalizer outputting said one of the potential digital signals to the ~~Viterbi~~ trellis decoder.

81. (currently amended) The integrated circuit communication device according to claim 80, wherein the characteristic feedback gain factor K is ramped to zero after convergence of the ~~decision~~ feedback equalizer circuitry.

82. (currently amended) The integrated circuit communication device according to claim ~~71~~ 79, the ~~single state decision~~ feedback equalizer circuitry having a set of ordered coefficients, the ~~decision~~ feedback equalizer circuitry defining a coefficient related tail value and a low order subset of coefficient values.

83. (currently amendedl) The integrated circuit communication device according to claim 82, wherein the ~~single state decision~~ feedback equalizer circuitry has a width dimension D, wherein the width dimension D corresponds to the number of pairs defining the multi-pair transmission channel.

84. (currently amended) The integrated circuit communication device according to claim 83, further comprising a state multiplication circuit, the state multiplication circuit expanding a single state representation output signal received from the ~~single state decision~~ feedback equalizer circuitry into an N-state representation signal suitable for decoding by the ~~DFSE~~ trellis decoder.

85. (original) The integrated circuit communication device according to claim 84, the state multiplication circuit comprising:

a convolution engine coupled to combine the low order subset of coefficient values with each member of a set of symbolic levels to define a fist sample signal set; and

a summing circuit coupled to combine the tail value with each member of the first sample signal set to define an N state representational set of signal samples.

86-159. (cancelled)